

Fig. 1

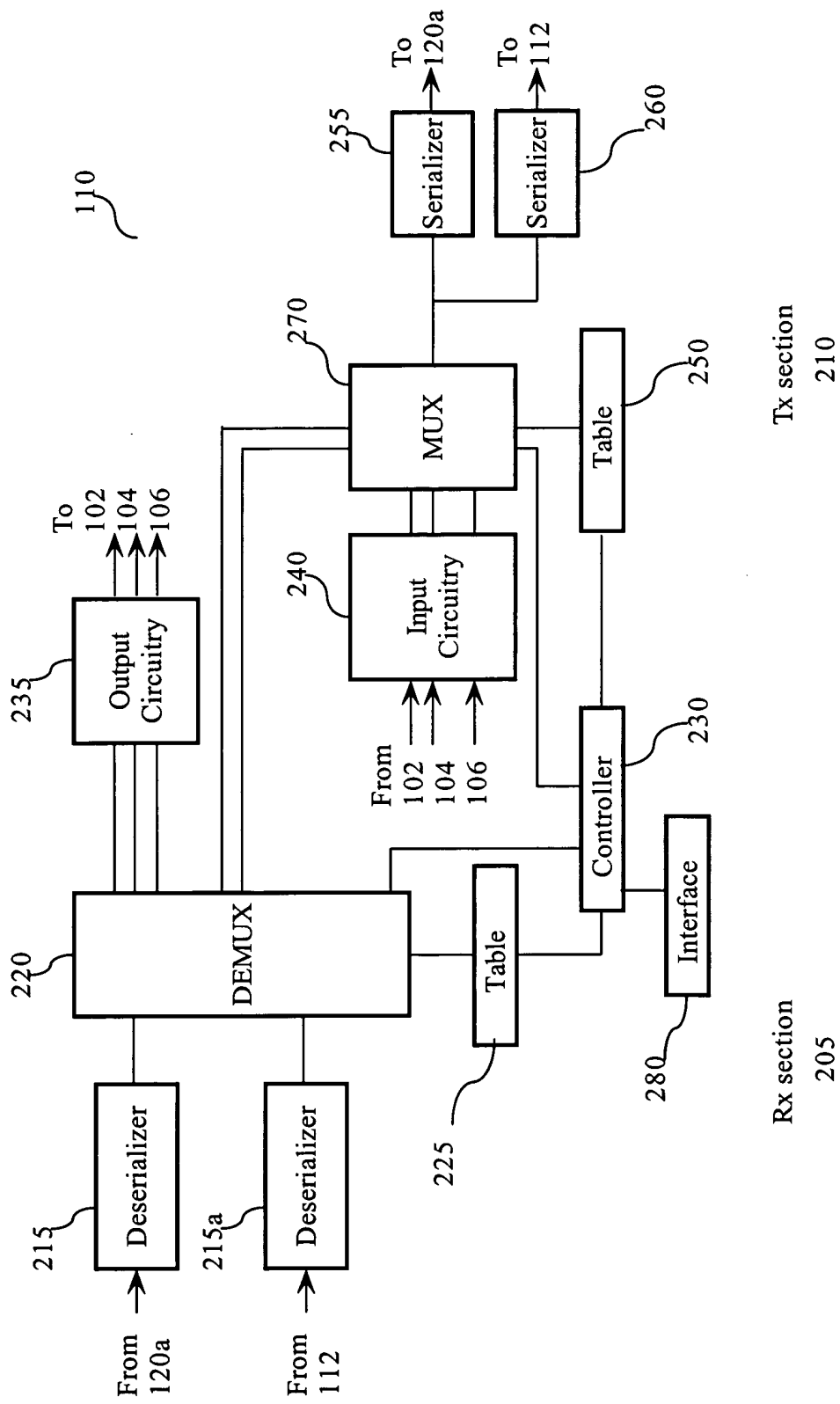


Fig. 2

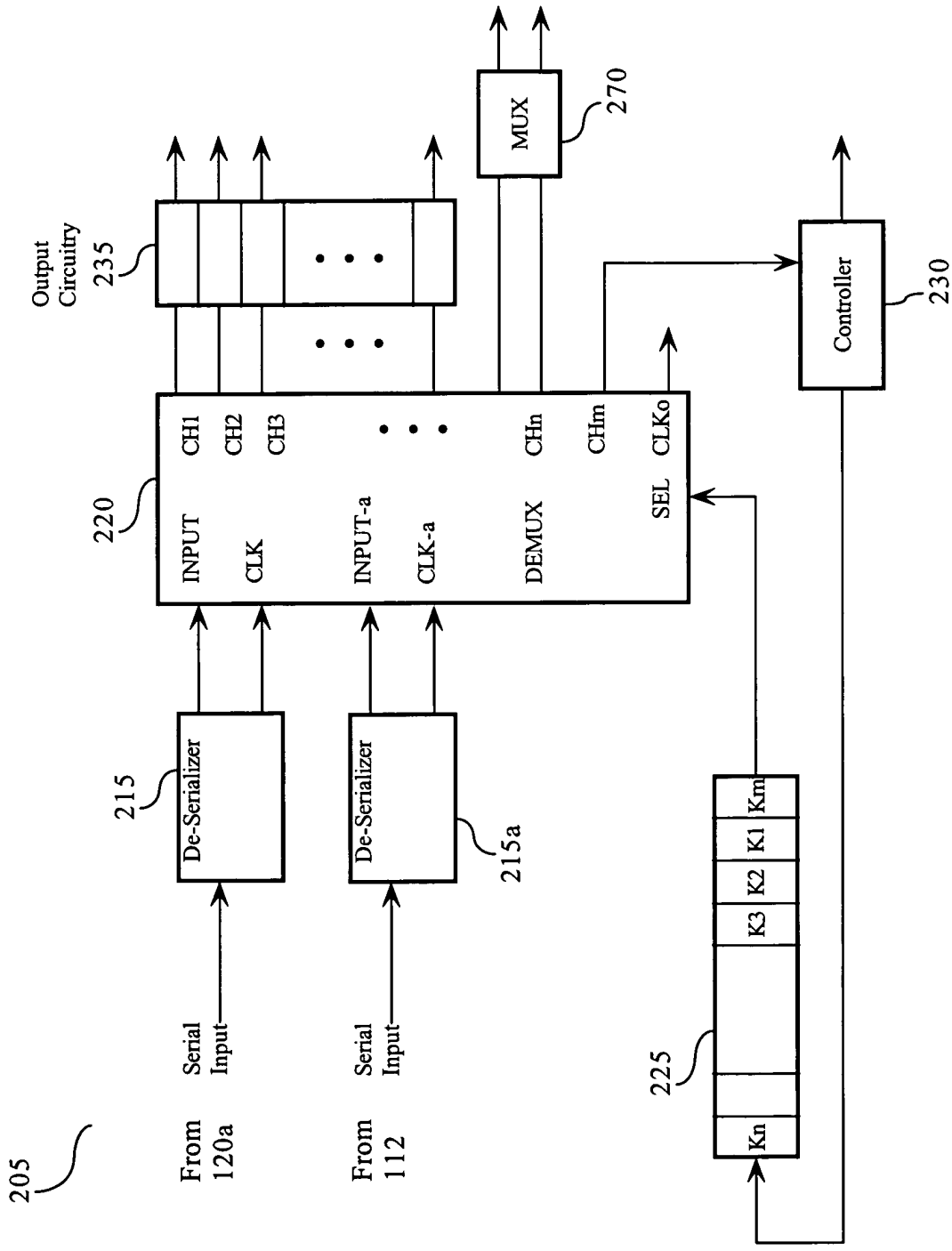


Fig. 3

235

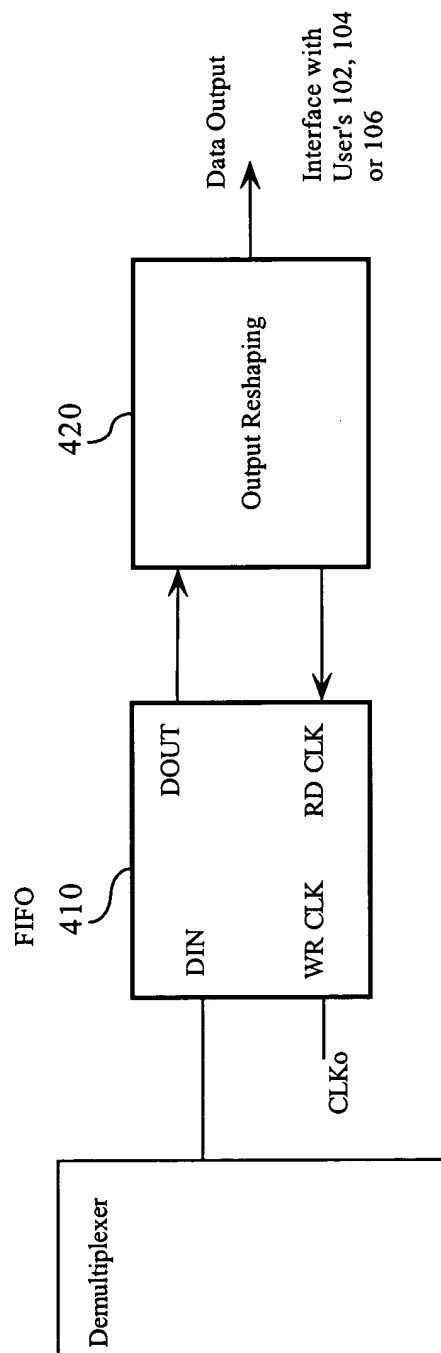


Fig. 4

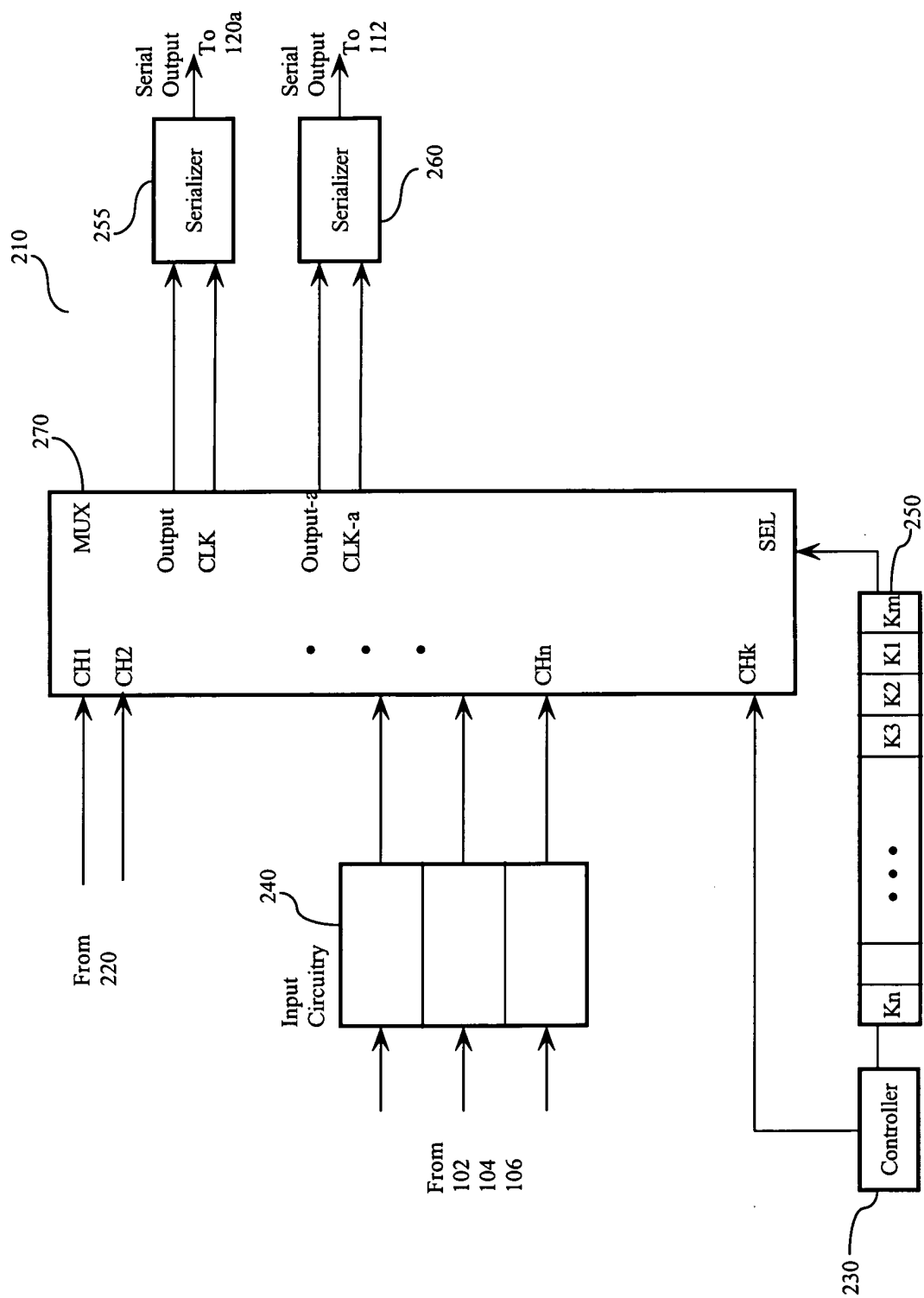


Fig. 5

FIG. 6 is a block diagram of a system 240. The system 240 includes a data input interface 102, 104, 106, an input reshap- ing block 640, a processing block 645, and a multiplexer 270. The data input interface 102, 104, 106 provides input to the input reshap- ing block 640. The input reshap- ing block 640 outputs to the processing block 645. The processing block 645 receives a write clock (WR CLK) and outputs a data output (DOUT) to the multiplexer 270. The multiplexer 270 also receives input from a channel input (CH i) and outputs to a channel output (CH o). The system 240 is clocked by a clock signal (CLKo) which is input to the processing block 645.

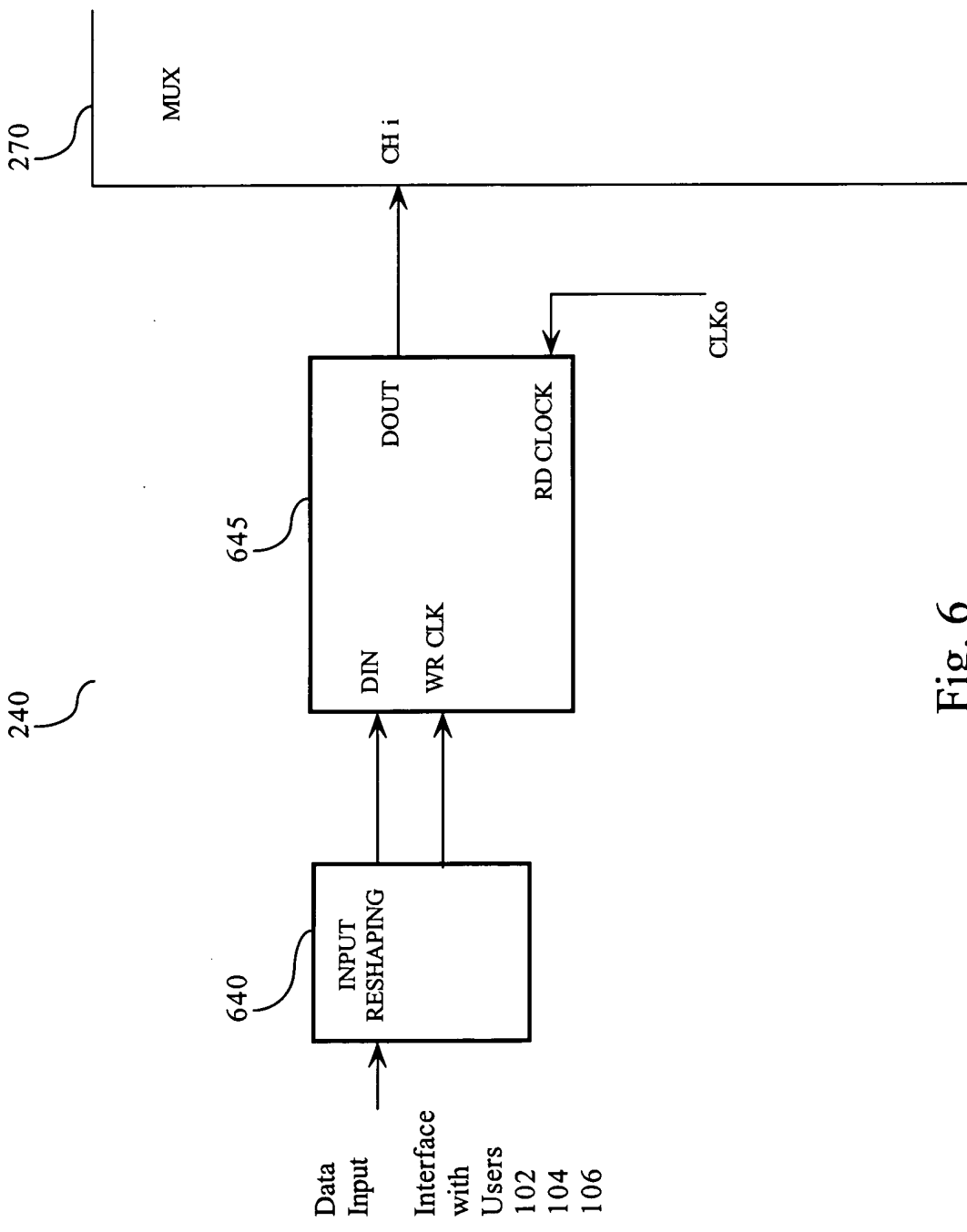


Fig. 6

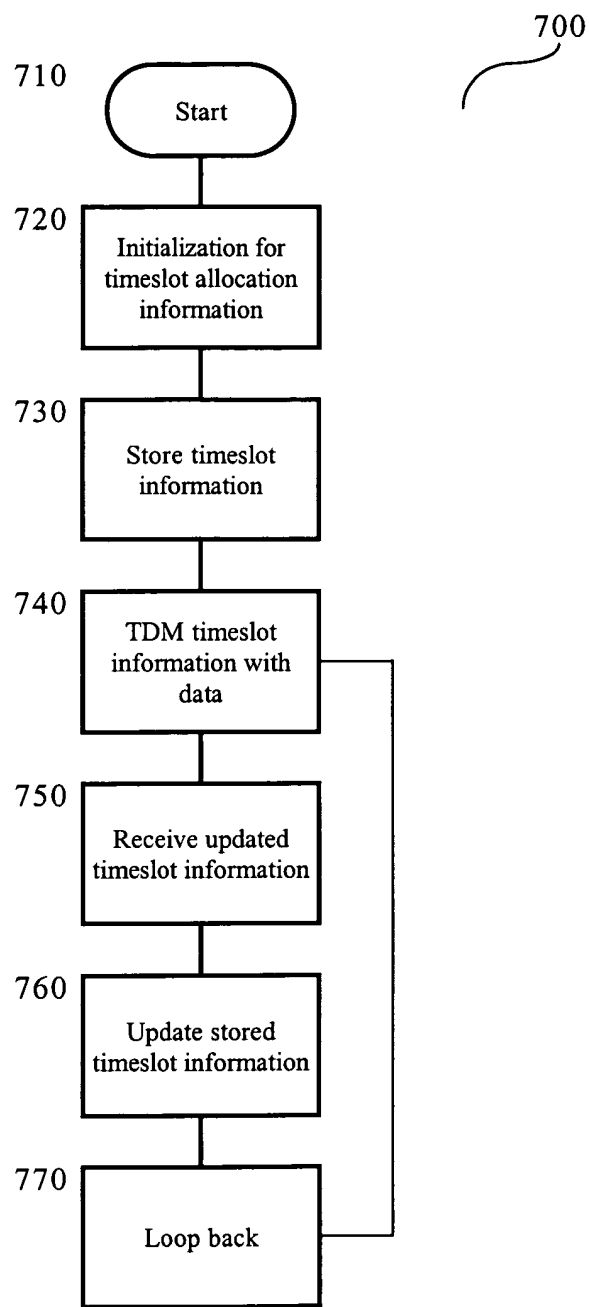


Fig. 7

	CHn	225 or 250	CH2	CH1	CHm
Clock Cycles	Kn	...	K2	K1	Km
Data Type		...			
Time Stamps		...			
Priority		...			
Sequence		...			
	<div> <div></div> <div></div> <div></div> </div>				
Inter-channel Relationship					

Fig.8